Total Ionizing Dose (TID) Test Report for the GARC ASIC

Testing Done February 2004, by Scott Kniffin and Lou Fetter.

A radiation evaluation was performed on the **GLAST ACD Readout Chip ASIC (GARC) (Agilent)** to determine the total dose tolerance of these parts. The total dose testing was performed using the Co^{60} gamma ray source at NASA GSFC Radiation Effects Facility. During the radiation testing, eight devices under test (DUTs) were irradiated under bias and one part was used as a control sample. The total dose radiation levels were 5, 7.5, and 10krads. The average dose rate was ~2.58rads(Si)/min (0.04rads(Si)/s). After the 10kRad irradiation, the parts were annealed under bias at 25?C for 168 hours. Due to issues described below, the devices were tested many times after this and had remained under bias at room temperature between measurements. After each radiation exposure and annealing treatment, parts were electrically tested according to the test conditions and the specification limits set by the project. An executive summary of the test results is provided below in bold, followed by a detailed summary of the test results after each radiation level and annealing step. The devices were biased on a custom etched board provided by the project in accordance with their needs and the application circuit. The devices were all marked the same: GLAST LAT GARC3-T36T ASAT NOV03 on the top and no markings on the bottom.

After significant post testing analysis, it was determined that all parts passed all tests up to 10krads. After annealing the parts at 25?C for 168 hours, there was no significant change noted in any parameter.

Initial electrical measurements were made on 9 samples. Eight samples (SN's 112, 113, 115, 116, 117, 118, 119, and 122) were used as radiation samples while SN 109 was used as a control sample. All parts passed all tests during initial electrical measurements.

After 10 krads(Si), some parameters appeared to have shifted beyond the specification limits given by the project. The "post 10krads(Si)" measurements were made several times over several days while maintaining the devices under bias at room temperature. Several more of these "failures" occurred after the 1-week annealing as well. After extensive examination of the test equipment and several more attempts to measure the electrical parameters of the devices, it was determined that the problems were the result of glitches in the test socket and not that of parametric degradation of the devices. Thus, all results were within the specifications given by the project, no significant changes were noted in any values.

After annealing the parts for 168 hours at 25?C, no significant change was noted in the measurements of any parameters after analyzing the data.

A total of 959 electrical measurements were taken on each device. Due to the number of parameters tested and the size of the data files, the measurements for each step are included in a separate spreadsheet to this report.

The data given in the spreadsheet should be interpreted as follows:
Pre-TID is the initial data taken on the devices; this is listed as pbi 25c on the spreadsheet. TID-1 corresponds to 5krads(Si) total dose, TID-2 corresponds to 7.5krads(Si) total dose, and TID-3 corresponds to 10krads(Si) total dose. Anneal corresponds to data taken after 168 hours of room temperature annealing and further annealing tests. The date of each test is given below the run name in row 4 of the spreadsheet in DDMMYYYY format. Parameters that tested out of specification are highlighted in the data columns.